FIG.1

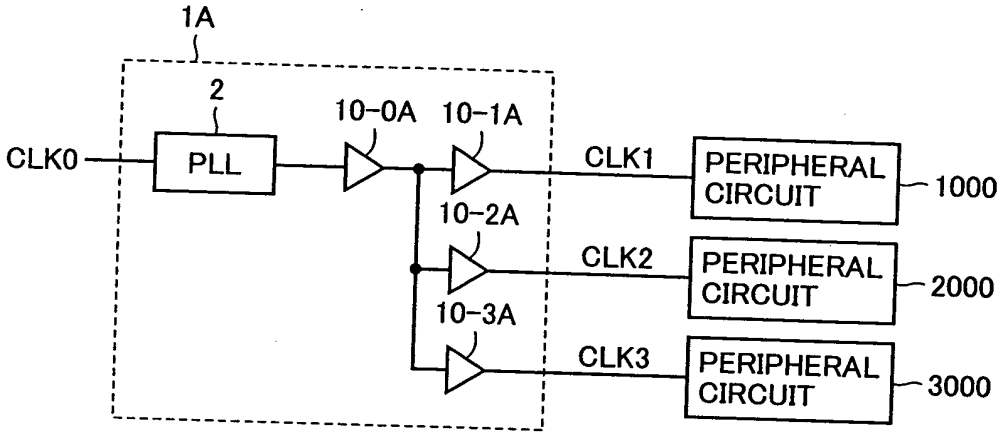

FIG.2

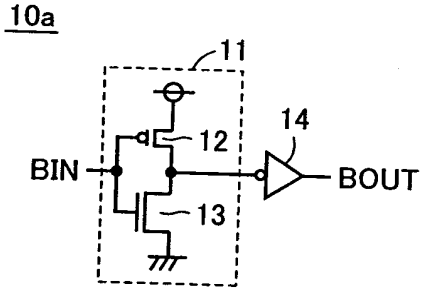

FIG.3

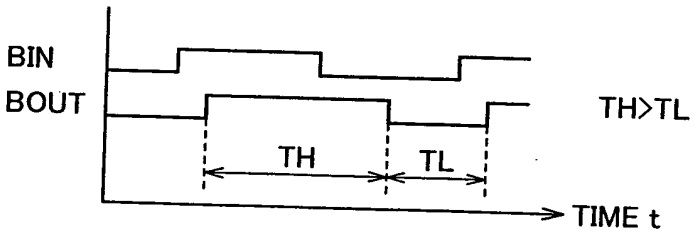

FIG.4

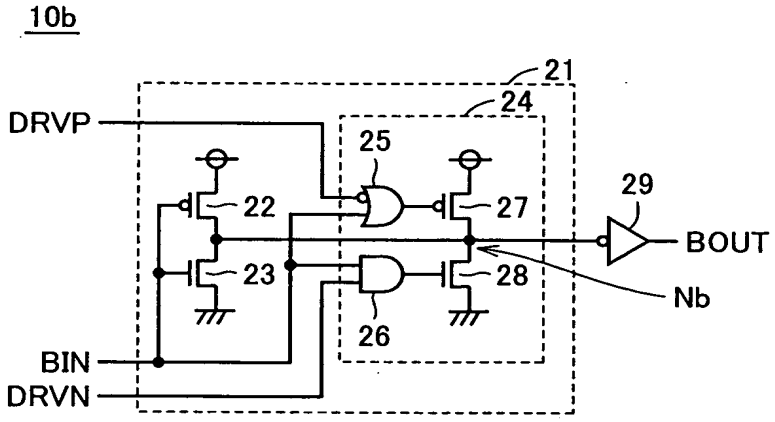

FIG.5

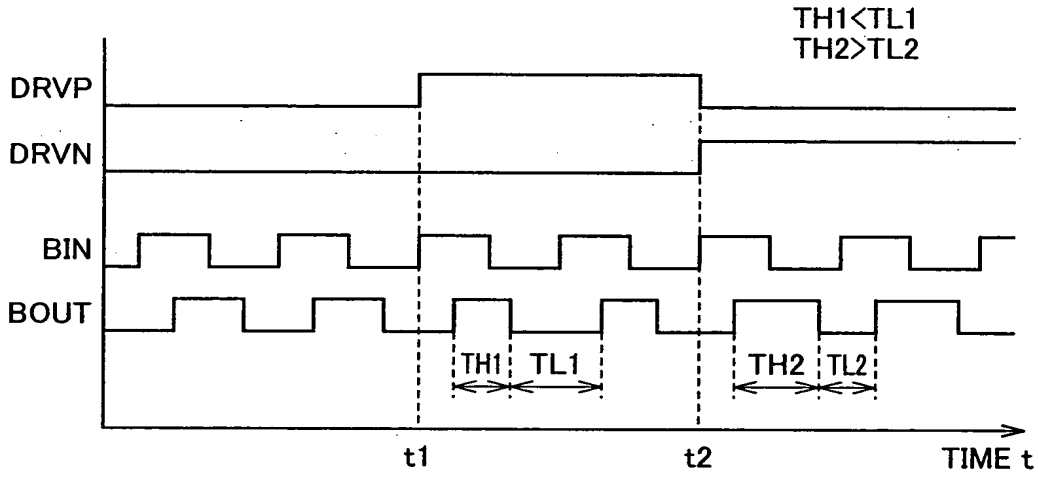

FIG.6

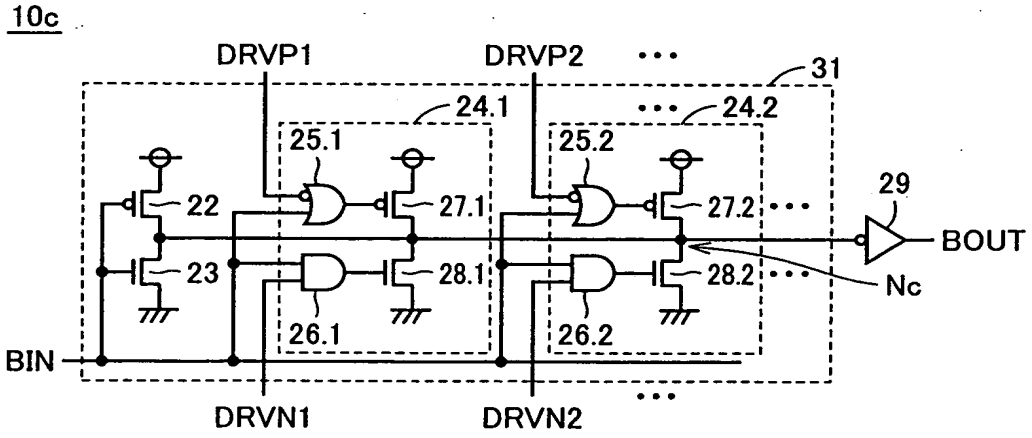

FIG.7

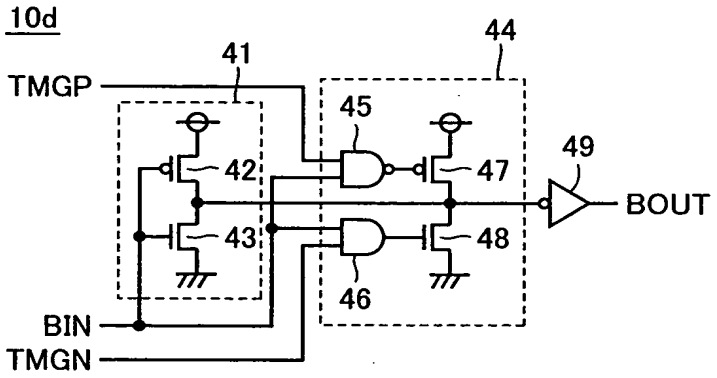

FIG.8

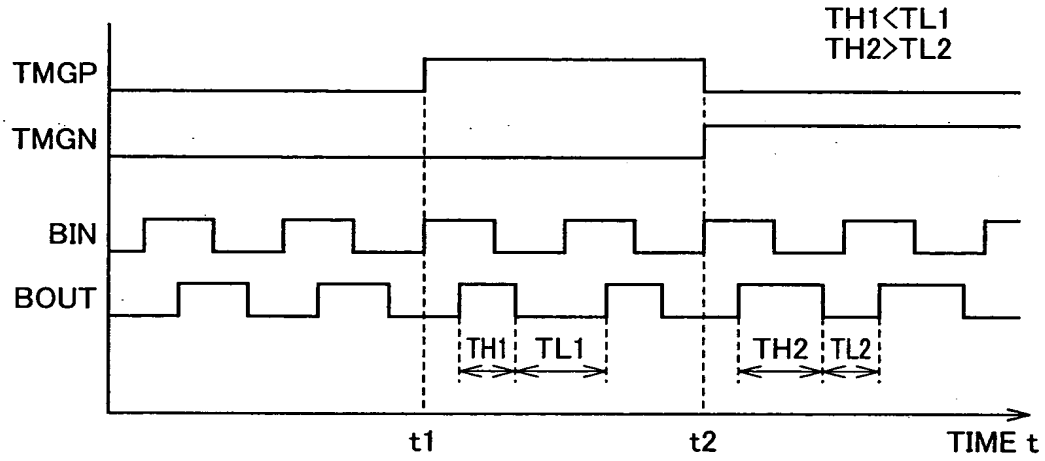

FIG.9

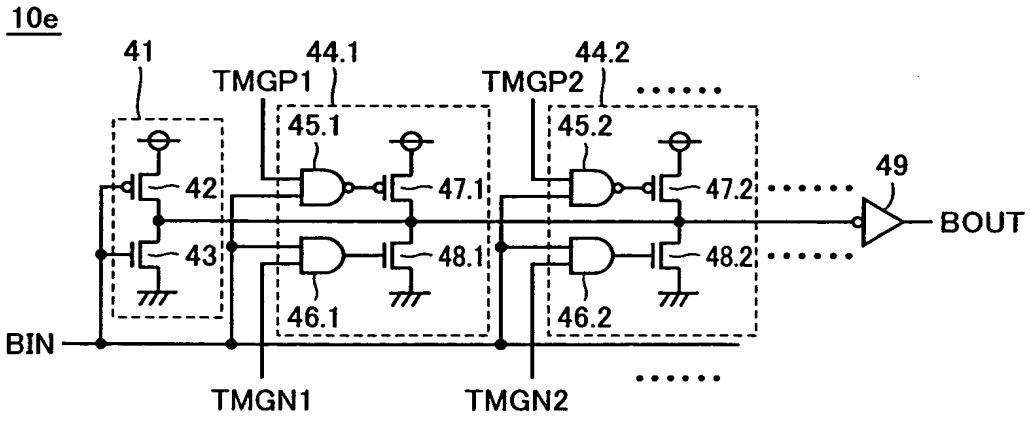

FIG.10

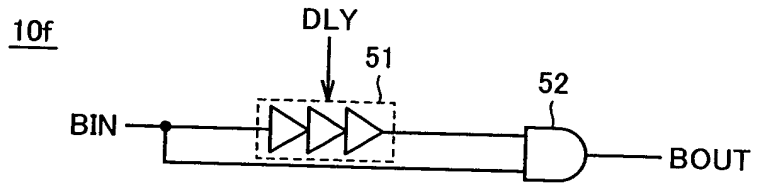
10f
DLY
51
52
BIN
BOUT

FIG.11

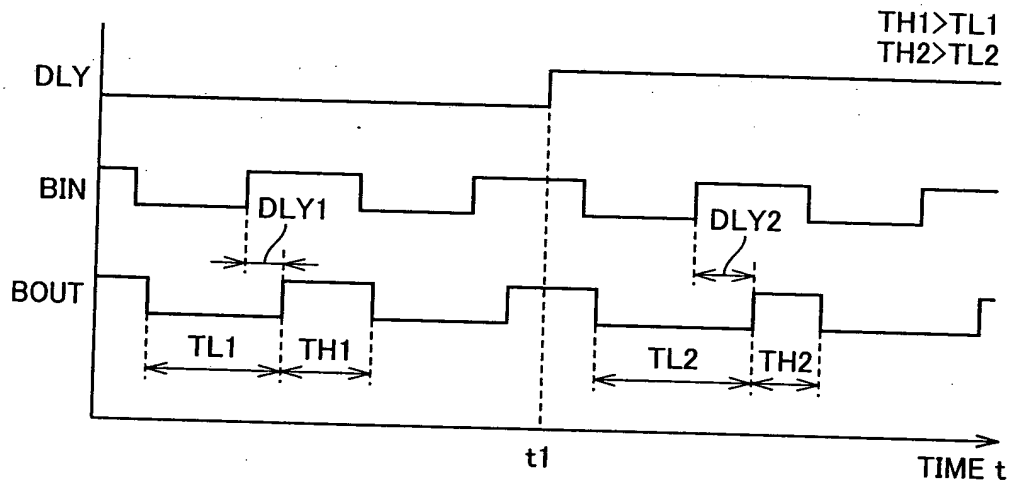
TH1>TL1
TH2>TL2
DLY
BIN
DLY1
DLY2
BOUT
TL1
TH1
TL2
TH2
t1
TIME t

FIG.12

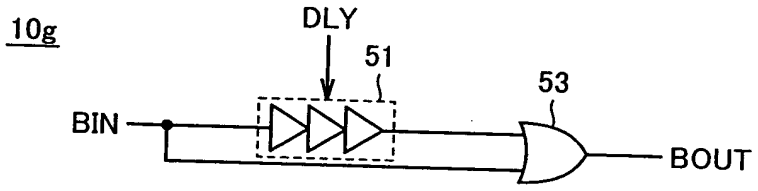
10g
DLY
51
53
BIN
BOUT

FIG.13

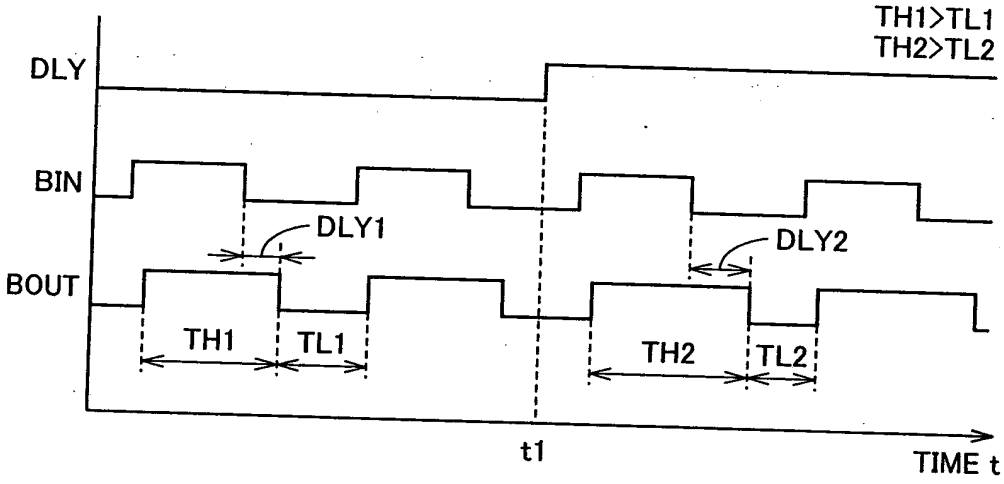
TH1>TL1
TH2>TL2
DLY
BIN
DLY1
DLY2
BOUT
TH1
TL1
TH2
TL2
t1
TIME t

FIG.14

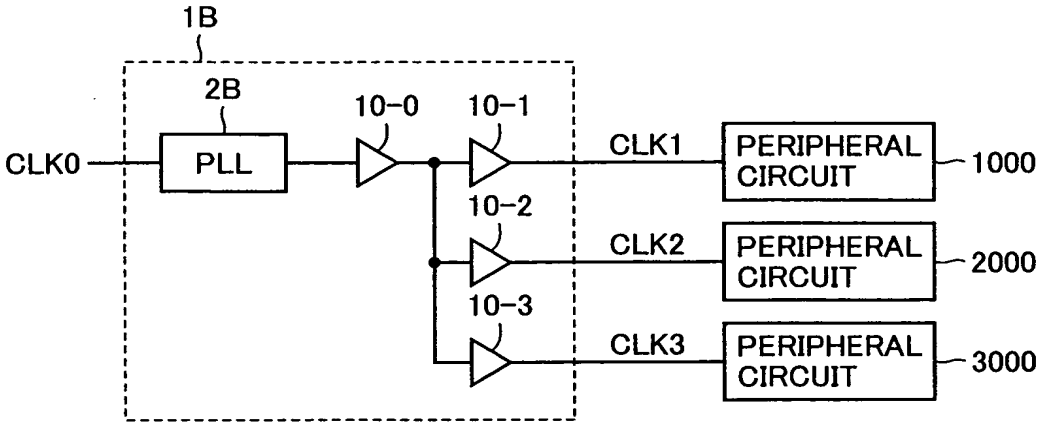

FIG.15

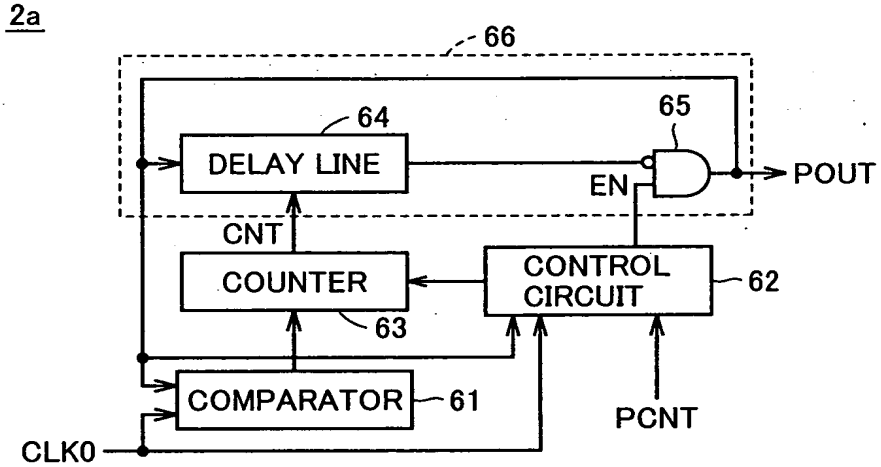

FIG.16

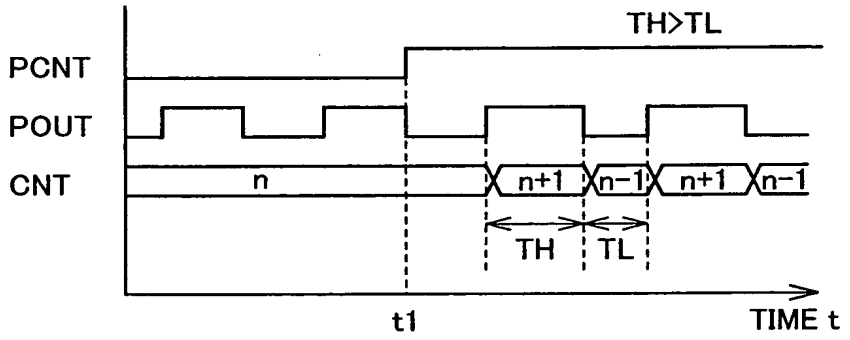

FIG.17

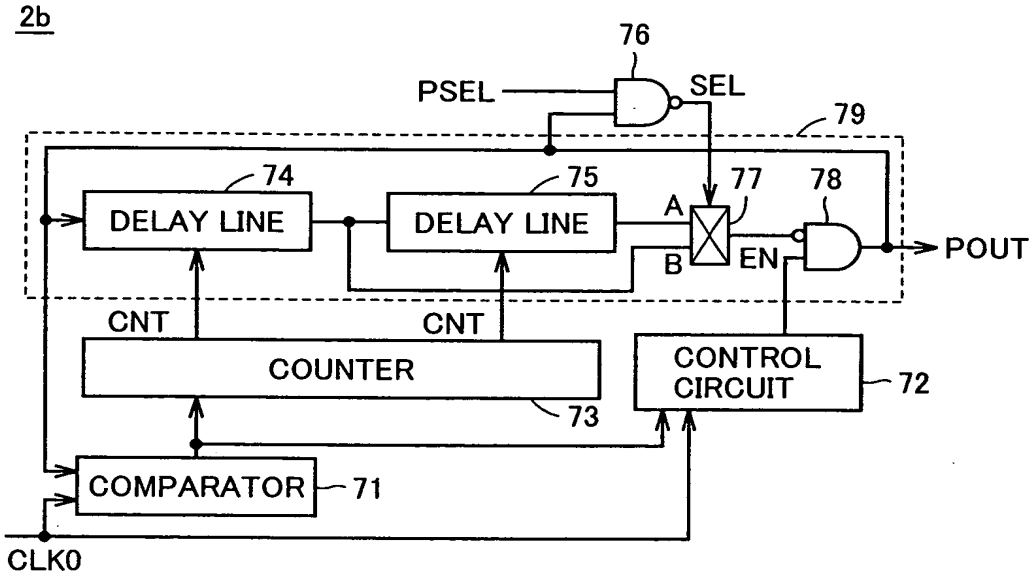
2b
76
PSEL
SEL
79
74
75
77
78
DELAY LINE
DELAY LINE
A
B
EN
POUT
CNT
CNT
COUNTER
73
CONTROL CIRCUIT
72
COMPARATOR
71
CLK0

FIG.18

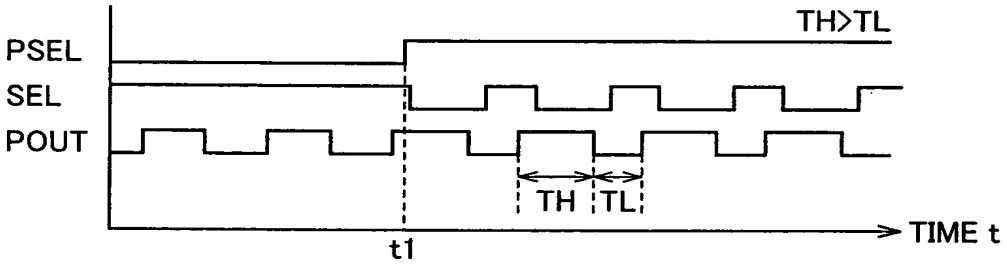
TH>TL
PSEL
SEL
POUT
TH
TL
TIME t
t1

FIG.19

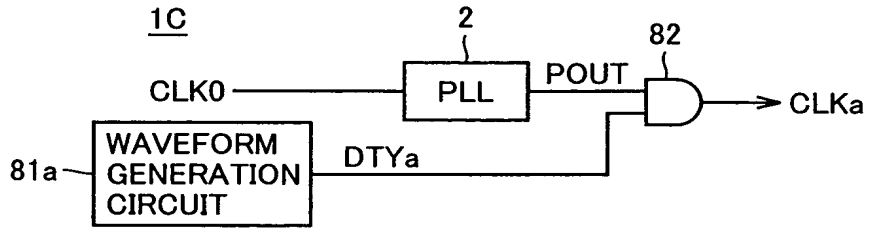

FIG.20

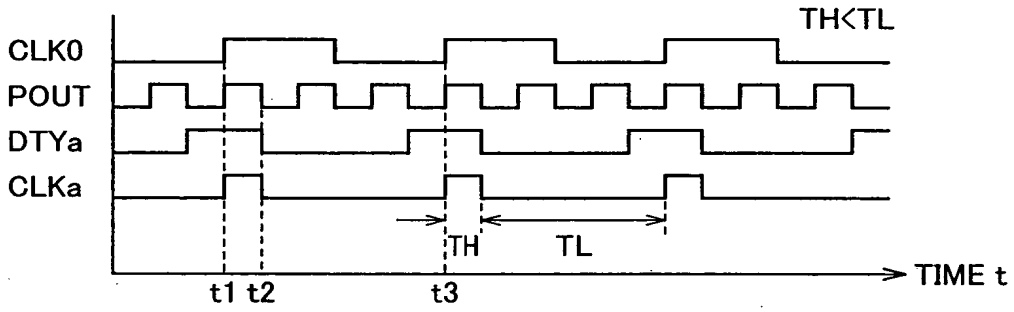

FIG.21

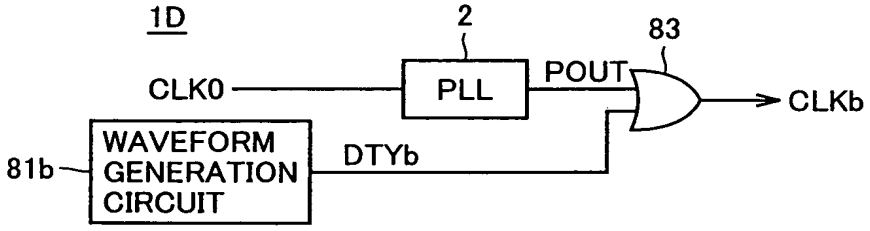

FIG.22

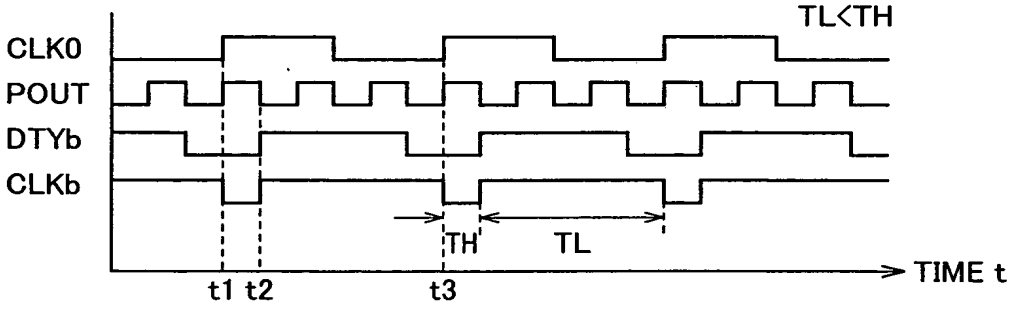

FIG.23

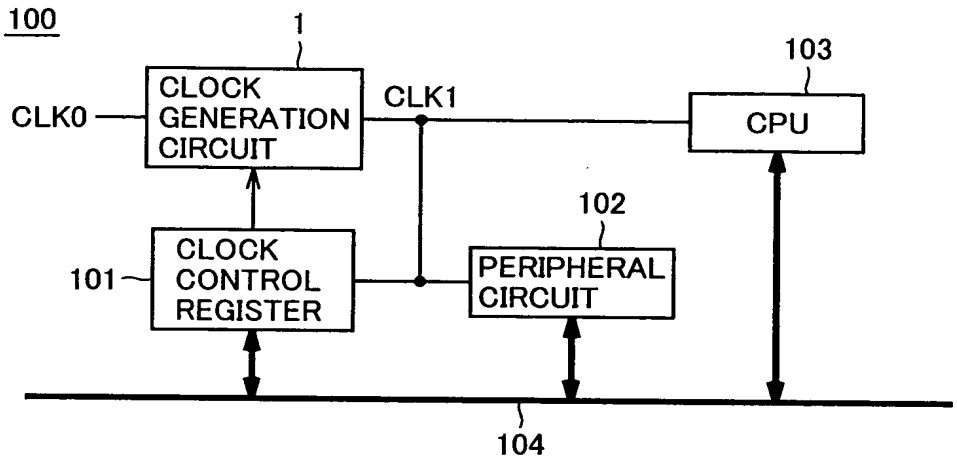
100
1
CLOCK GENERATION CIRCUIT
CLK0
CLK1
103
CPU
102
CLOCK CONTROL REGISTER
101
PERIPHERAL CIRCUIT
104

FIG.24

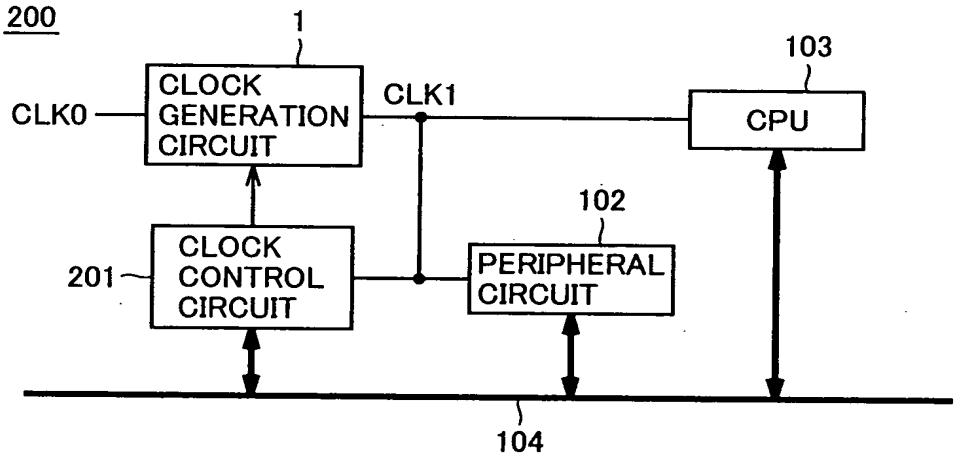
200
1
CLOCK GENERATION CIRCUIT
CLK0
CLK1
103
CPU
102
CLOCK CONTROL CIRCUIT
201
PERIPHERAL CIRCUIT
104

FIG.25

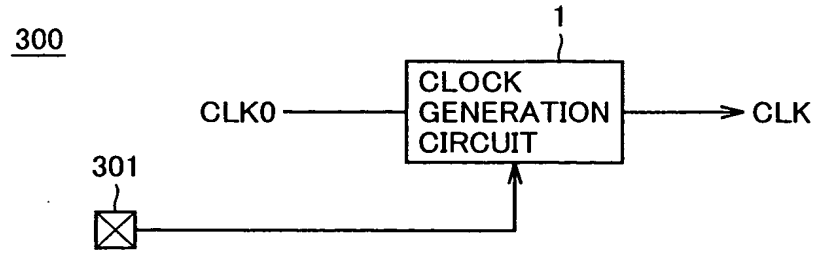

FIG.26

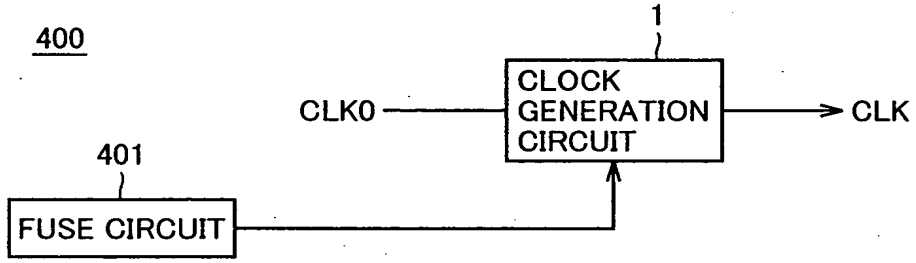

FIG.27

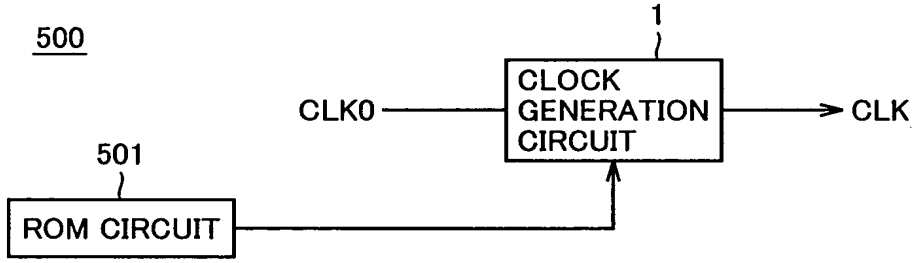
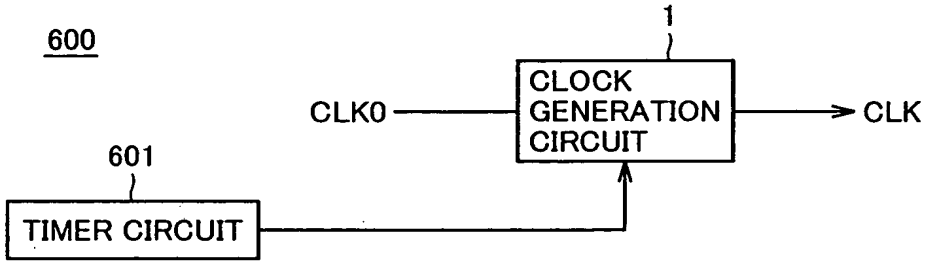
FIG.28